

[0090] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A semiconductor device comprising:  
  
source and drain regions provided in a SOI substrate, said source and drain regions being of a first conductivity type; and  
  
a gate structure on said SOI substrate and between said source and drain regions, said gate structure being of a second conductivity type.
2. The semiconductor device of claim 1, wherein said first conductivity type is n-type and said second conductivity type is p-type.
3. The semiconductor device of claim 1, wherein said first conductivity type is p-type and said second conductivity type is n-type.
4. The semiconductor device of claim 1, wherein said gate structure comprises a doped polysilicon layer.
5. The semiconductor device of claim 1, wherein said gate structure comprises a doped silicon/germanium layer.
6. The semiconductor device of claim 1, wherein said gate structure comprises a metal gate layer.
7. The semiconductor device of claim 4, wherein said gate structure further comprises a silicide layer over said doped polysilicon layer.
8. The semiconductor device of claim 1, wherein the conductivity doping of said gate structure causes said semiconductor device to be a fully-depleted SOI NMOS transistor.

9. The semiconductor device of claim 8, wherein said fully-depleted SOI NMOS transistor is an access transistor for a memory cell.

10. The semiconductor device of claim 8, wherein said fully-depleted SOI NMOS transistor is part of a memory array.

11. The semiconductor device of claim 1, wherein the conductivity doping of said gate structure causes said semiconductor device to be a fully-depleted SOI PMOS transistor.

12. The semiconductor device of claim 11, wherein said fully-depleted SOI PMOS transistor is an access transistor for a memory cell.

13. A memory device comprising:

a SOI substrate; and

at least one fully-depleted memory cell access transistor comprising a gate stack fabricated on said SOI substrate, said gate stack having a first conductivity type, and source and drain regions of a second conductivity type formed in said SOI substrate and disposed adjacent said gate stack.

14. The memory device of claim 13, wherein said first conductivity type is n-type and said second conductivity type is p-type.

15. The memory device of claim 13, wherein said first conductivity type is p-type and said second conductivity type is n-type.

16. The memory device of claim 13, wherein said gate stack comprises a doped polysilicon layer.

17. The memory device of claim 13, wherein said gate stack comprises a doped silicon/germanium layer.

18. The memory device of claim 16, wherein said gate stack further comprises a silicide layer over said doped polysilicon layer.

19. The memory device of claim 13, wherein said fully-depleted access transistor is a fully-depleted SOI NMOS transistor.

20. The memory device of claim 19, wherein said fully-depleted SOI NMOS transistor is part of a memory array.

21. The memory device of claim 13, wherein said memory device is a DRAM device.

22. The memory device of claim 13, wherein said fully-depleted access transistor is a fully-depleted SOI PMOS transistor.

23. A memory cell comprising:

a plurality of gate stacks over a SOI substrate, at least one of said plurality of gate stacks comprising a polysilicon layer of a first conductivity type;

source/drain regions in said SOI substrate on opposite sides of each of said plurality of gate stacks, at least one of said source/drain regions being of a second conductivity type and being disposed adjacent said at least one of said plurality of gate stacks comprising said polysilicon layer of said first conductivity type; and

a storage device connected to one of said source/drain regions.

24. The memory cell of claim 23, wherein said first conductivity type is n-type and said second conductivity type is p-type.

25. The memory cell of claim 23, wherein said first conductivity type is p-type and said second conductivity type is n-type.

26. The memory cell of claim 23, wherein said at least one of said plurality of gate stacks comprising said polysilicon layer of said first conductivity type further comprises a silicide layer over said polysilicon layer.

27. A processor-based system comprising:

a processor; and

an integrated circuit coupled to said processor, at least one of said integrated circuit and processor comprising a transistor, said transistor comprising:

source and drain regions provided on a SOI substrate, said source and drain regions being of a first conductivity type; and

a gate stack fabricated on said SOI substrate, said gate stack including a conductive layer of a second conductivity type.

28. The processor-based system of claim 27, wherein said transistor is a fully-depleted SOI transistor.

29. The processor-based system of claim 28, wherein said fully-depleted SOI transistor is a fully-depleted SOI NMOS transistor.

30. The processor-based system of claim 27, wherein said first conductivity type is n-type and said second conductivity type is p-type.

31. The processor-based system of claim 27, wherein said first conductivity type is p-type and said second conductivity type is n-type.

32. The processor-based system of claim 27, wherein said conductive layer is a doped polysilicon layer.

33. The processor-based system of claim 27, wherein said conductive layer is a doped silicon/germanium layer.

34. The processor-based system of claim 27, wherein said gate structure further comprises a silicide layer over said conductive layer.

35. The processor-based system of claim 27, wherein said gate structure further comprises a cap layer over said conductive layer.

36. A semiconductor device comprising:

a SOI substrate;

at least one partially-depleted MOSFET device of a first conductivity type on a periphery region of said SOI substrate; and

at least one fully-depleted MOSFET device of the first conductivity type on a memory array region of said SOI substrate, said fully-depleted MOSFET device further comprising a gate structure of a second conductivity type.

37. The semiconductor device of claim 36, said first conductivity type is n-type and said second conductivity type is p-type.

38. The semiconductor device of claim 36, wherein said first conductivity type is p-type and said second conductivity type is n-type.

39. The semiconductor device of claim 36, wherein said partially-depleted MOSFET device is a partially-depleted NMOS transistor and said fully-depleted MOSFET device is a fully-depleted NMOS access transistor.

40. The semiconductor device of claim 36, wherein said gate structure comprises a doped polysilicon layer.

41. The semiconductor device of claim 36, wherein said gate structure comprises a doped silicon/germanium layer.

42. The semiconductor device of claim 40, wherein said gate structure further comprises a silicide layer over said doped polysilicon layer.

43. A method of forming at least one gate structure of a transistor comprising the acts of:

providing a doped conductive layer of a first conductivity type over a SOI substrate;

forming at least one gate stack over said SOI substrate, said gate stack comprising a portion of said doped conductive layer; and

forming source and drain regions of a second conductivity type on opposite sides of said gate stack.

44. The method of claim 43, wherein said first conductivity type is n-type and said second conductivity type is p-type.

45. The method of claim 43, wherein said first conductivity type is p-type and said second conductivity type is n-type.

46. The method of claim 43, wherein said act of providing said doped conductive layer further comprises subjecting a conductive layer to a first implantation with a dopant of said first conductivity type.

47. The method of claim 46, wherein said first implantation is conducted at an energy of about 1keV to about 50keV.

48. The method of claim 47, wherein said first implantation is further conducted at a dose concentration of about  $1 \times 10^{15}/\text{cm}^2$  to about  $5 \times 10^{15}/\text{cm}^2$ .

49. The method of claim 43 further comprising the act of providing an oxide layer on said SOI substrate before said act of providing said doped conductive layer.

50. The method of claim 49 further comprising the act of providing a silicide layer over said doped conductive layer.

51. The method of claim 50 further comprising the act of providing dielectric cap layer over said silicide layer.

52. The method of claim 51, wherein said act of forming said gate stack further includes the act of patterning said doped conductive layer, said silicide layer and said dielectric cap layer.

53. The method of claim 51, wherein said act of forming said gate stack further includes the act of etching said doped conductive layer, said silicide layer and said dielectric cap layer to form said gate stack.

54. The method of claim 49 further comprising the act of forming spacers on sidewalls of said gate stack.

55. The method of claim 54, wherein said act of forming source and drain regions further comprises the act of subjecting said gate stack to a second implantation with a dopant of said second conductivity type.

56. The method of claim 55, wherein said second implantation is conducted at an energy of about 1keV to about 60keV.

57. The method of claim 56, wherein said second implantation is further conducted at a dose concentration of about  $1 \times 10^{14}/\text{cm}^2$  to about  $5 \times 10^{15}/\text{cm}^2$ .

58. A method of forming a fully-depleted SOI NMOS transistor comprising the acts of:

forming an oxide layer over a SOI substrate;

forming a doped polysilicon layer of p-type conductivity over said oxide layer;

forming a gate stack comprising portions of said oxide layer and of said doped polysilicon layer; and

forming source and drain region of n-type conductivity on opposite sides of said gate stack.

59. The method of claim 58, wherein said act of providing said doped polysilicon layer further comprises subjecting a polysilicon layer to a first implantation with a p-type dopant.

60. The method of claim 59, wherein said first implantation is conducted at an energy of about 1keV to about 50keV.

61. The method of claim 60, wherein said first implantation is further conducted at a dose concentration of about  $1 \times 10^{15}/\text{cm}^2$  to about  $5 \times 10^{15}/\text{cm}^2$ .

62. The method of claim 58, wherein said oxide layer is formed by thermally oxidizing said SOI substrate.

63. The method of claim 58 further comprising the act of providing a silicide layer over said doped polysilicon layer.

64. The method of claim 63 further comprising the act of providing a dielectric cap layer over said silicide layer.

65. The method of claim 64, wherein said act of forming said gate stack further includes the act of patterning said doped polysilicon layer, said silicide layer and said dielectric cap layer.

66. The method of claim 65, wherein said act of forming said gate stack further includes the act of etching said doped polysilicon layer, said silicide layer and said dielectric cap layer to form said gate stack.

67. The method of claim 58 further comprising the act of forming spacers on sidewalls of said gate stack.

68. The method of claim 67, wherein said act of forming source and drain regions further comprises the act of subjecting said gate stack to a second implantation with an n-type dopant.

69. The method of claim 68, wherein said second implantation is conducted at an energy of about 1keV to about 60keV.

70. The method of claim 69, wherein said second implantation is further conducted at a dose concentration of about  $1 \times 10^{14}/\text{cm}^2$  to about  $5 \times 10^{15}/\text{cm}^2$ .

71. A method of forming a semiconductor device comprising the acts of:  
providing a SOI substrate;

forming at least one isolation region in said SOI substrate for separating at least one periphery region of said SOI substrate from at least one memory array region of said SOI substrate;

forming at least one partially-depleted SOI MOSFET device of a first conductivity type in said periphery region of said SOI substrate; and

forming at least one fully-depleted SOI MOSFET device of said first conductivity type in said memory array region of said SOI substrate, said fully-depleted SOI MOSFET device comprising a gate electrode of a second conductivity type.

72. The method of claim 71, wherein said first conductivity type is n-type and said second conductivity type is p-type.

73. The method of claim 71, wherein said first conductivity type is p-type and said second conductivity type is n-type.

74. The method of claim 71, wherein said gate electrode of said fully-depleted SOI MOSFET device is formed of a doped conductive layer provides over said memory array region.

75. The method of claim 74 further comprising the act of subjecting said conductive layer to a first implantation with a dopant of said second conductivity type.

76. The method of claim 75, wherein said first implantation is conducted at an energy of about 1keV to about 50keV.

77. The method of claim 76, wherein said first implantation is further conducted at a dose concentration of about  $1 \times 10^{14}/\text{cm}^2$  to about  $5 \times 10^{15}/\text{cm}^2$ .

78. The method of claim 74 further comprising the act of providing an oxide layer on said memory array region of said SOI substrate before said act of providing said doped conductive layer.

79. The method of claim 78 further comprising the act of providing a silicide layer over said doped conductive layer.

80. The method of claim 79 further comprising the act of providing a dielectric cap layer over said silicide layer.

81. The method of claim 80, wherein said act of forming said fully-depleted SOI MOSFET device further includes the act of patterning said doped conductive layer, said silicide layer and said dielectric cap layer formed over said memory array region.

82. The method of claim 81, wherein said act of forming said fully-depleted SOI MOSFET device further includes the act of etching said doped conductive layer, said silicide layer and said dielectric cap layer to form a gate stack.

83. The method of claim 82 further comprising the act of forming source and drain regions on opposite sides of said gate stack and in said memory array region.

84. The method of claim 83, wherein said act of forming source and drain regions further comprises the act of subjecting said gate stack to a second implantation with a dopant of said second conductivity type.

85. The method of claim 84, wherein said second implantation is conducted at an energy of about 1keV to about 60keV.

86. The method of claim 85, wherein said second implantation is further conducted at a dose concentration of about  $1 \times 10^{14}/\text{cm}^2$  to about  $5 \times 10^{15}/\text{cm}^2$ .